AP 2817

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: FENG LIN	Group Art Unit: 2817
Serial No.: 10/623,959	Examiner: CHANG, JOSEPH
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For: A PHASE DETECTOR FOR REDUCING NOISE	CUSTOMER NO. 23720

APPEAL BRIEF

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8	
DATE OF DEPOSIT:	April 3, 2006
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Sir:

On January 27, 2006, Appellants filed a Notice of Appeal in response to a Final Office Action dated October 27, 2005, issued in connection with the above-identified application. In support of the appeal, Appellants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences.

Since the Notice of Appeal for the present invention was received and stamped by the USPTO Mailroom on February 1, 2006, the two-month date for filing this Appeal Brief is April 1, 2006. Since April 1, 2006 falls on a Saturday, this Appeal Brief is being mailed on Monday, April 3, 2006, therefore, it is timely filed.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

The Commissioner is authorized to deduct the fee for filing this Appeal Brief ($500.00) from Williams, Morgan & Amerson, P.C., Deposit Account No. 50-0786/2008.007700. No other fee is believed to be due in connection with the filing of this document. However, should any fee under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to this document, the Commissioner is hereby authorized to deduct said fee from Williams, Morgan & Amerson, P.C., Deposit Account No. 50-0786/2008.007700.

I. REAL PARTY IN INTEREST

The present application is owned by Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF CLAIMS

Claims 1-13 remain pending in this application. Claims 1, 2 and 7-13 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,744,293 ***(Fu)*** for reasons of record. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Fu*** for reasons of record. Claim 3 is objected to.

IV. STATUS OF AMENDMENTS

Claim 1 was amended in the Final Rejection dated December 22, 2005 to address an informality, and that amendment was acknowledged by the Examiner in the Advisory Action dated January 18, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

One or more embodiments of the present invention are generally directed to synchronization of periodic signals, such as clock signals. More particular embodiments are directed to a phase detector for reducing noise in an apparatus employing periodic signals. The Background Section of the Patent Application explains one or more shortcomings in the prior art where series of adjustments of alternating "up" and "down" signals may create noise, thereby affecting the stability of the device relying on clock signals. To reduce, or at least address, the shortcomings of the prior art system(s), the Patent Application describes an apparatus that employs a phase detector in an arrangement that is specified in the various pending claims. Against this general backdrop, one or more of the embodiments are discussed.

Figure 1 shows a simplified block diagram of a digital system 100. The digital system 100 includes a digital device 105 coupled to a second digital device 110. The digital device 105 provides a reference clock signal (CLKIN) to the second digital device 110. The second digital device 110 uses the CLKIN signal to synchronize its internal clocks using a delay locked loop 115 and generate an output clock signal (CLKOUT). As an illustrative example, the second

digital device 110 may be a memory device that synchronizes its output data on a data line 120 with the CLKOUT signal. Patent Application, p. 6, ll. 14-23.

Figure 2 illustrates one embodiment of the delay locked loop 115 that receives the CLKIN signal and provides the CLKOUT signal. In the illustrated embodiment, the CLKIN signal and a FEEDBACK signal are provided to a phase detector 200, which may determine a phase difference between the CLKIN signal and the FEEDBACK signal. Patent Application, p. 7, ll. 1-8.

The phase detector 200 provides one or more signals indicative of the phase difference between the CLKIN signal and the FEEDBACK signal to a control logic 210. In the illustrated embodiment, the phase detector 200 provides a binary output based on the relative phase difference between the CLKIN and FEEDBACK signals. For example, the phase detector 200 may provide a shift-left signal (SL) if the FEEDBACK signal leads the CLKIN signal and a shift-right signal (SR) if the FEEDBACK signal lags the CLKIN signal. Patent Application, p. 7, ll. 10-15.

In the illustrated embodiment, the control logic 210 includes a shift register 215 that may receive the shift-left signal (SL) or the shift-right signal (SR). The CLKIN signal is provided to an adjustable delay 220 in the delay locked loop 115. In one embodiment, the adjustable delay 220 includes a plurality of delay elements 225(1-n). Each of the delay elements 225(1-n) may be capable of introducing a unit time delay into the CLKIN signal. For example, the delay elements 225(1-n) may each be a digital device, such as a NAND gate (not shown) and the like,

that may introduce a unit time delay of about 200 picoseconds into the CLKIN signal. Patent Application, p. 7, ll. 16-24.

The delay locked loop 115 may also include a delay 230. The control logic 210 is coupled to the adjustable delay 220. In the illustrated embodiment, the control logic 210, may provide a signal to the adjustable delay 220 that may be used to select one or more of the delay elements 225(1-n). An adjustable delay 220 may be introduced into the CLKIN signal by providing the CLKIN signal to the one or more selected delay elements 225(1-n). In one embodiment, the control logic 210 may select one or more of the delay elements 225(1-n) to compensate for the delay 230 such that the CLKIN signal is approximately in phase with the CLKOUT signal. For example, if the delay locked loop 115, has an intrinsic delay of about 3.5 nanoseconds and the period of the CLKIN signal is about 5 nanoseconds, then seven delay elements 225(1-n), each having a unit time delay of about 200 picoseconds, may be selected by the control logic 210. In the illustrated embodiment, the control logic 210 may select the one or more delay elements 225(1-n) using information stored in the shift register 215. Patent Application, p. 8, ll. 1-14.

The phase detector 200 may detect a phase difference between the CLKIN signal and the FEEDBACK signal that is less than about one unit time delay, which may result in the phase detector 200 providing an adjustment signal, such as a shift-left signal (SL) and/or a shift-right signal (SR), to the control logic 210. The adjustable delay 220 may over-adjust the CLKIN signal by introducing a time delay of at least one unit time delay into the CLKIN signal. The over-adjusted CLKIN signal may be provided to the phase detector 200 via the FEEDBACK

path, which may detect the new phase difference between the CLKIN signal and the FEEDBACK signal and provide a compensating adjustment signal to the control logic 210. However, the FEEDBACK signal may be delayed by approximately the delay 230. Thus, to reduce the number of undesirable adjustment signals that may be provided to the control logic 210, and thereby reduce noise and improve the loop stability of the delay locked loop 115, a CONTROL signal may be used in one embodiment of the phase detector 200, as illustrated in Figure 3. Patent Application, p. 8, ll. 16-24.

In the illustrated embodiment, the phase detector 200 includes a hysteresis adjuster 300, a phase detector core 310, and a digital filter 320. The hysteresis adjuster 300, which is described in detail below, receives the CLKIN signal and the FEEDBACK signal and provides modified signals, CLKIN' and FEEDBACK', to the phase detector core 310. Patent Application, p. 10, ll. 8-16.

The phase detector core 310 generates a signal that is indicative of the phase difference between the CLKIN' signal and the FEEDBACK' signal. In the illustrated embodiment, the phase detector core 310 generates an UP signal to indicate that the CLKIN' signal leads the FEEDBACK' signal and a DOWN signal to indicate that the CLKIN' signal lags the FEEDBACK' signal. The phase detector core 310 provides the UP and DOWN signal to the digital filter 320, which may use the UP and DOWN signals to respectively generate the shift-left signal (SL) and the shift-right signal (SR). In one embodiment, the digital filter 320 may be a majority filter that may provide a signal in response to detecting at least two consecutive determined phase differences in the same direction. For example, the digital filter 320 may

provide a shift-left signal (SL) in response to receiving two consecutive UP signals and a shift-right signal (SR) in response to receiving two consecutive DOWN signals. Patent Application, p. 10, l. 18 – p. 11, l. 8.

The digital filter 320 also provides a CONTROL signal to the hysteresis adjuster 300. In one embodiment, the CONTROL signal is not filtered by the digital filter 320. For example, the CONTROL signal may correspond to the UP and/or DOWN signals provided to the digital filter 320 by the phase detector core 310. The hysteresis adjuster 300 may provide modified signals, CLKIN' and FEEDBACK', in response to receiving the CONTROL signal, as described below. Patent Application, p. 11, ll. 9-15.

Figure 4 shows one embodiment of the hysteresis adjuster 300, which includes a fixed delay 400 and an adjustable delay 410. In one embodiment, the fixed delay 400 forms the CLKIN' signal by introducing a predetermined time delay into the CLKIN signal. For example, the fixed delay 400 may include two delay elements (not shown) to introduce a predetermined time delay of about two unit delays into the CLKIN signal. Patent Application, p. 11, ll. 16-24.

The adjustable delay 410 may introduce a selected time delay into the FEEDBACK signal to form the FEEDBACK' signal. In one embodiment, the time delay is selected in response to receiving the CONTROL signal. If the CONTROL signal corresponds to the DOWN signal, the selected time delay may be larger than the time delay introduced by the fixed delay 400. For example, if the fixed delay 400 introduced a time delay of about two unit delays, the adjustable delay 410 may introduce a selected time delay of about three unit delays into the

FEEDBACK signal. If the CONTROL signal corresponds to the UP signal, a selected time delay may be about equal to the time delay introduced by the fixed delay 400. For example, if the fixed delay 400 introduced a time delay of about two unit delays, the adjustable delay 410 may also introduce a selected time delay of about two unit delays into the FEEDBACK signal. Patent Application, p. 12, ll. 1-12.

To illustrate the operation of the phase detector 200, consider the following example. Initially, the CLKIN signal is assumed to lag the FEEDBACK signal by less than about one unit time delay. The fixed delay 400 and the adjustable delay 410 are further assumed to introduce equal time delays into the CLKIN signal and the FEEDBACK signal, respectively. Thus, the CLKIN' signal initially lags the FEEDBACK' signal by less than about one unit time delay. The phase detector core 310 then determines that the CLKIN' signal lags the FEEDBACK' signal and provides a DOWN signal to the digital filter 320. As discussed above, in this embodiment, the digital filter 320 is a majority filter. Assuming that this is the first DOWN signal received by digital filter 320, no shift-left signal (SL) or shift-right signal (SR) is provided by the digital filter 320, and the adjustable delay 220 shown in Figure 2 remains unchanged. Patent Application, p. 12, ll. 14-24.

The digital filter 320 also provides the CONTROL signal indicative of the DOWN signal to the hysteresis adjuster 300. In response to receiving the CONTROL signal indicative of the DOWN signal, the adjustable delay 410 introduces a delay into the FEEDBACK signal that is larger than the delay introduced into the CLKIN signal by the fixed delay 400. For example, if the delay introduced by the fixed delay 400 is approximately two unit delays, then the adjustable

delay 410 will introduce a delay of approximately three unit delays in response to receiving the CONTROL signal indicative of the DOWN signal. Patent Application, p. 13, ll. 10-16.

The delay introduced by the adjustable delay 410 results in the CLKIN' signal leading the FEEDBACK' signal by less than about one time delay unit during the next clock cycle, assuming that the phase difference between the CLKIN signal and the FEEDBACK signal remained approximately constant. Thus, the phase detector core 310 provides an UP signal to the digital filter 320. Since the previous signal received by the digital filter 320 was a DOWN signal, no shift-left signal (SL) or shift-right signal (SR) is provided by the digital filter 320, and the adjustable delay 220 shown in Figure 2 remains unchanged. Patent Application, p. 13, ll. 10-16.

In response to receiving the CONTROL signal indicative of the UP signal, the adjustable delay 410 reduces the delay introduced into the FEEDBACK signal so that is about equal to the delay introduced into the CLKIN signal by the fixed delay 400. For example, if the delay introduced by the fixed delay 400 is approximately two unit delays, then the adjustable delay 410 will introduce a delay of approximately two unit delays in response to receiving the CONTROL signal indicative of the UP signal. Consequently, the CLKIN' signal will now lag the FEEDBACK' signal by less than one time delay unit during the next clock cycle, assuming that the phase difference between the CLKIN signal and the FEEDBACK signal remained approximately constant. Patent Application, p. 13, ll. 18-24.

As illustrated by the previous example, differences between the CLKIN signal and the FEEDBACK signal that are less than about one unit time delay may not result in a shift-left

signal (SL) or a shift-right signal (SR) being provided by the digital filter 320, so that the adjustable delay 220 shown in Figure 2 remains unchanged. The loop stability of the phase detector 200 may therefore be increased by including the hysteresis adjuster 300, the phase detector core 310, and the digital filter 320. Furthermore, by increasing the loop stability of the phase detector 200 in the manner described above, undesirable jitter in the output clock signal may be reduced, thereby increasing the stability of the digital devices 105, 110 relying on the output clock and reducing errors that may be caused by jitter of the output clock signal. Patent Application, p. 14, ll. 4-14.

Illustrative input and output signals for two embodiments of the phase detector 200 are shown in Figures 5A and 5B. It will be appreciated by those of ordinary skill in the art that the illustrated signals are exemplary in nature and are not intended to limit the present invention. Figure 5A shows two simulated input signals 500 having a small phase difference. It will be appreciated that the coarse resolution of Figure 5A, and the small phase difference between the two input signals 500, causes the two input signals 500 to blend together so that they appear as a single line. Figure 5A also shows a simulated output signal 505 for a phase detector, such as the phase detector 200 shown in Figure 2, without a hysteresis adjuster 300 or a filter, such as the hysteresis adjuster 300 and the digital filter 320 shown in Figure 3. A simulated output signal 510 for a phase detector core, such as the phase detector core 310 shown in Figure 3, is also shown in Figure 5A. Patent Application, p. 14, ll. 15-24.

Figure 5B shows two simulated input signals 520 having a small phase difference. It will be appreciated that the coarse resolution of Figure 5B, and the small phase difference between

the two input signals 520, causes the two input signals 520 to blend together so that they appear as a single line. Figure 5B also shows a simulated output signal 525 for a phase detector, such as the phase detector 200 shown in Figure 2, having a hysteresis adjuster and a filter, such as the hysteresis adjuster 300 and the digital filter 320 shown in Figure 3. A simulated output signal 530 for a phase detector core, such as the phase detector core 310 shown in Figure 3, is also shown. Patent Application, p. 15, ll. 4-11.

By comparing the simulated signals shown in Figures 5A and 5B, persons of ordinary skill in the art will appreciate that undesirable jitter in the simulated output signal 505 produced by the phase detector 200 that does not include a hysteresis adjuster 300 and a filter 320 is reduced in the simulated output signal 525 produced by the phase detector 200 having the hysteresis adjuster 300 and the filter 320. Patent Application, p. 15, ll. 13-17.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether Claim 1 and its dependent claims are anticipated by U.S. Patent 6,744,293 ***(Fu)***?

2. Whether Claim 2 is anticipated by U.S. Patent 6,744,293 ***(Fu)***?

3. Whether Claim 10 is anticipated by U.S. Patent 6,744,293 ***(Fu)***?

4. Whether Claim 11 is anticipated by U.S. Patent 6,744,293 ***(Fu)***?

5. Whether Claims 13 is anticipated by U.S. Patent 6,744,293 ***(Fu)***?

6. Whether Claims 4-6 are patentable over ***Fu*** and US Patent No. 6,198,326 (***Choi***)?.

VII. ARGUMENT

A. Claims 1 and its dependent claims are Patentable over Fu

Independent claim 1 and its dependent claims are allowable over Fu. Claim 1 is directed to an apparatus that calls for a phase detector adapted to determine a phase difference between at least two input signals. Claim 1, among other things, also calls for a second circuit adapted to receive a first signal, to receive a second signal, and to modify the second signal based upon the control signal. The reference to a "first signal" and "modified signal" makes clear that claim 1 calls for at least two signals. Claim 1 further specifies that the second circuit is adapted to provide these two signals as the input signals to the phase detector. Thus, when this last claimed feature is read in light of the first claimed feature (i.e., a phase detector adapted to determine a phase difference between at least two input signals), it is clear that claim 1 calls for the phase detector to determine a phase difference between the first signal and the modified second signal that are provided to it as the two input signals.

The Examiner argues that claim 1 is anticipated Fu. The Examiner's arguments are without merit for several reasons, as discussed below.

The Examiner asserts that Fu discloses providing two signals to the phase detector 106 from the clock buffer 104 (see Figure 1 of Fu). In particular, the Examiner argues that the "first signal" of claim 1 corresponds to signal 103 of Fu, and the "modified signal" corresponds to signal 109. *See* Office Action, pages 2-3. The Examiner further argues that the modified signal 109 of Fu becomes signal 103 and, consequently, both are input signals to the phase detector 106. *See* Office Action, page 3. In other words, the Examiner is arguing that clock buffer 104

itself provides two signals to the phase detector. The Examiner's application of Fu is problematic for several reasons.

First, notwithstanding the Examiner's assertion, even a cursory review of Fu reveals that only one signal (and not two) from the clock buffer 104 is provided to the phase detector 106. The Examiner appears to rely solely on the graphical illustration of Figure 1, rather than the description of Figure 1 in Fu, to make his rejection. The actual textual description in Fu, however, directly undercuts the Examiner's argument and reveals that only one, rather than two signals, is provided to the phase detector 106 from clock buffer 104. In particular, Fu discloses, at col. 2, liens 28-33, that the "phase detector 106 includes a first input connected to an output of the clock buffer 104 for receiving an offset incoming clock signal." Thus, Fu clarifies that the phase detector 106 receives the offset incoming clock signal. Fu does not state, as the Examiner alleges, that a second signal is received from clock buffer 104. The only other signal received by the phase detector 106 is on another input line, in particular, from the local reference clock signal line 101, and not from the clock buffer 104. Thus, notwithstanding the Examiner's assertions, Fu specifies that are the phase detector 106 receives only one signal from the clock buffer 104, and not two different signals as called for by claim 1.

More importantly, even assuming that two signals are provided by the clock buffer 104 (as alleged by the Examiner), the Examiner's argument nevertheless fails for another fundamental reason. As noted above, when read in its entirety, claim 1 calls for a phase detector adapted to determine a phase difference between the first signal and the modified signal. Under the Examiner's application of Fu, the phase detector 106 would have to determine the phase

difference between signals 103 and 109, and it does not. Rather, Fu teaches that the phase detector 106 determines the phase difference between the outputs of the clock buffer 104 and clock VDU 102. Fu, col. 2, lines 28-33; col. 2, lines 18-23. Thus, even under the Examiner's flawed application of Fu, Fu still does not teach a detector that is adapted to determine a phase difference between the first signal and the modified signal.

B. Claim 2 Is Patentable Over Fu

Claim 2, which depends from claim 1, is allowable for at least the reasons claim 1 is allowable, and is further allowable for the additional feature recited therein. Claim 2 specifies wherein the second circuit is adapted to modify the first signal before providing the modified first signal to the phase detector. The Examiner does not even attempt to address claim 2 in any of the Office Actions.

Claim 2, when read in the context of its independent claim 1, it calls for modifying the second signal (claim 1) and modifying the first signal (claim 2) before providing it to the phase detector. The Examiner is unable to explain what two signals in Fu are modified before they are applied to the phase detector 106. The Examiner thus has failed to meet his burden of establishing anticipation with respect to claim 2.

C. Claim 10 Is Patentable Over Fu

Claim 10 is allowable for at least the reasons its independent claim 1 is allowable. Moreover, claim 10 is also allowable because the Examiner has not shown how claim 10 is anticipated by Fu in any of the three preceding Office Actions, including the June 1, 2005 Office Action, August 27, 2005 Final Office Action, and June 18, 2006 Advisory Action. Accordingly,

claim 10 is allowable in view of the Examiner's failure to establish a prima face case of anticipation.

D. Claim 11 Is Patentable Over Fu

Claim 11 is allowable for at least the reasons its independent claim 1 is allowable. Moreover, claim 11 is also allowable because it recites an additional feature not taught or suggested by Fu. Claim 11 specifies wherein the first circuit is a majority filter adapted to provide a signal indicative of the desired clock signal delay *in response to at least two consecutive determined phase differences in the same direction.* With respect to claim 11, the Examiner argues that "the digital filter 108 is inherently performing the functional recitation." *See* Office Action, June 1, 2005, page 3. Here, the Examiner simply makes a conclusory statement, and offers absolutely no scientific reasoning to establish the reasonableness of the examiner's belief that the functional recitation (i.e., "adapted to provide a signal ... *in response to at least two consecutive determined phase differences in the same direction*") is an inherent characteristic of the prior art. The Examiner's uncorroborated statement is clearly improper under the legal precedent.

It is well-established that inherency in anticipation requires that the asserted proposition *necessarily* flow from the disclosure. *In re Oelrich*, 212 U.S.P.Q. (BNA) 323, 326 (C.C.P.A. 1981); *Levy*, 17 U.S.P.Q.2d (BNA) at 1463-64; *Skinner*, at 1789; *In re King*, 231 U.S.P.Q. (BNA) 136, 138 (Fed. Cir. 1986). It is not enough that a reference could have, should have, or would have been used as the claimed invention. "The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Oelrich*, at 326, quoting *Hansgirg v. Kemmer*, 40 U.S.P.Q. (BNA) 665, 667 (C.C.P.A. 1939); *In re Rijckaert*, 28 U.S.P.Q.2d (BNA)

1955, 1957 (Fed. Cir. 1993), quoting *Oelrich*, at 326; *see also Skinner*, at 1789. "Inherency... may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Ex parte Skinner*, 2 U.S.P.Q.2d (BNA) 1788, 1789 (Bd. Pat. App. & Int. 1987), citing *In re Oelrich*, 666 F.2d 578, 581 (C.C.P.A. 1981).

In the instant case, the Examiner's asserted proposition does not *necessarily* flow from the disclosure. That is, the filter 108 in Fu does not necessarily provide a signal in response to at least two consecutive determined phase differences in the same direction, as called for by claim 11. To the contrary, Fu indicates otherwise. In particular, Fu describes that the filer 108 controls the amount of delay based on the phase differences in either (i.e., not necessarily the same) direction based on the output of the phase detector 200 (detector 106 in Figure 1). Fu, 3:51-65 (describing the different outputs from the filter 108 when either the "lag" or "lead" output signal from the detector 106/200 is "high"). Thus, the Examiner's inherency rejection is not only based on an unsupported statement, it is inconsistent with the teachings of Fu, the very reference relied upon by the Examiner.

E. Claim 13 Is Patentable Over Fu

Claim 13 is allowable for at least the reasons its independent claim 1 is allowable. Moreover, claim 13 is also allowable because it recites an additional feature not taught or suggested by Fu. Claim 13 specifies wherein the second circuit of claim 1 comprises a hysteresis adjuster. The term "second circuit" in claim 13 derives its antecedent basis from claim 1 (as evident by the presence of the term "the" before the term "second circuit"). As such, the

"second circuit" referenced in claim 13 is the same circuit referenced in the independent claim. However, as explained below, the Examiner inconsistently applies Fu to claim 13 and its independent claim (claim 1) in an attempt to sustain the anticipation rejection. Such a rejection is clearly improper.

To understand the flaw in the Examiner's argument, it is first helpful to recall how the Examiner applies Fu to claim 1. In rejecting claim 1, the Examiner argues that the combination of the clock buffer 104 and clock VDU 102 corresponds to the "second circuit" of claim 1. *See* Office Action, June 1, 2005, p. 2. To consistently apply Fu across both claims, claims 1 and 13, the Examiner must thus show that the clocks 102, 104 (i.e., "second circuit," according to the Examiner) include the hysteresis adjuster specified in claim 13. Fu, however, includes no such teaching or suggestion.

Even the Examiner does not contend that clocks 102, 104 of Fu include the hysteresis adjuster. Rather, the Examiner argues that the hysteresis adjuster is shown in the lock detector 110 of Fu. Office Action, June 1, 2005, page 3. However, the lock detector 110 is not the "second circuit" according to the Examiner. The "second circuit" corresponds to the clocks 102, 104 under the Examiner's application of Fu to claim 1. Thus, Fu at least does not teach the second circuit comprising a hysteresis adjuster. Accordingly, claim 13 is allowable for this additional reason.

F. Claims 4-6 Are Patentable Over Fu and Choi

Claims 4-6 are allowable for at least the reasons their independent claim 1 is allowable. Moreover, these claims also allowable because the Examiner has failed to establish a prima facie case of obviousness.

With respect to claims 4-6, the Examiner rejects these claims under 35 U.S.C. 103(a) as being unpatentable over Fu. It is not entirely clear from the Final Office Action if the Examiner also relies on Choi to make the obviousness rejection. Although the Examiner makes a passing reference to Choi on page 3 of the Final Office Action, the introductory section entitled "Claim Rejections – 35 USC § 103" indicates that the Examiner is relying solely on Fu for the rejection. To the extent the Examiner relies only on Fu, the Examiner has failed to provide an **affidavit** in accordance with **37 C.F.R. § 1.104(d)(2)**. Moreover, the Examiner has failed to provide the requisite motivation to combine and the reasonable expectation of success that is necessary to establish a prima facie case of obviousness.

To the extent that Examiner is now relying on Choi to substantiate his obviousness rejection, the Applicants respectfully note that the Examiner has failed to establish a prima facie case of obviousness. Like Fu, Choi also fails to teach one or more of the claim features discussed above. Additionally, the Examiner has failed to establish the requisite motivation to combine the references in the manner suggested and also failed to show the expectation of success. Accordingly, claims 4-6 are allowable for these additional reasons.

VIII. CLAIMS APPENDIX

The claims currently under consideration, *i.e.*, claims 1, 2 and 4-13, are listed in the Claims Appendix. Claim 3 is objected to, but is otherwise deemed allowable.

IX. EVIDENCE APPENDIX

There is no evidence relied upon in this Appeal with respect to this section.

X. RELATED PROCEEDINGS APPENDIX

There are no related appeals and/or interferences that might affect the outcome of this proceeding.

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing the claims (claims 1, 2, and 4-13) pending in the present application over the prior art of record. The undersigned attorney may be contacted at (713) 934-4064 with respect to any questions, comments, or suggestions relating to this appeal.

Respectfully submitted,
WILLIAMS, MORGAN & AMERSON, P.C.

Date: 4/3/06

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1. (Previously Amended) An apparatus, comprising:

a phase detector adapted to determine a phase difference between at least two input signals;

a first circuit adapted to generate a control signal based upon the determined phase difference; and

a second circuit adapted to:

receive a first signal;

receive a second signal;

modify the second signal based upon the control signal; and

provide the first signal and the modified second signal as the input signals to the phase detector.

2. (Previously Amended) The apparatus of claim 1, wherein the second circuit is adapted to modify the first signal before providing the modified first signal to the phase detector.

3. (Previously Amended) The apparatus of claim 2, wherein the second circuit is adapted to provide the modified first signal and the modified second signal as input signals to the phase detector, and wherein the phase detector is adapted to determine a phase difference between the modified first signal and the modified second signal.

4. (Original) The apparatus of claim 1, wherein the second circuit comprises a fixed delay and an adjustable delay.

5. (Original) The apparatus of claim 4, wherein the fixed delay comprises at least one delay element.

6. (Original) The apparatus of claim 4, wherein the adjustable delay comprises at least two delay elements, at least one of the delay elements in the adjustable delay being selectable based upon the control signal.

7. (Original) The apparatus of claim 1, wherein the phase detector is capable of providing a signal indicative of the determined phase difference to the first circuit.

8. (Previously Amended) The apparatus of claim 7, wherein the signal indicative of the determined phase difference is a binary signal.

9. (Original) The apparatus of claim 8, wherein the control signal is a binary control signal formed using the binary phase difference signal.

10. (Original) The apparatus of claim 1, wherein the first circuit is adapted to provide a signal indicative of a desired clock signal delay based upon the determined phase difference.

11. (Original) The apparatus of claim 1, wherein the first circuit is a majority filter adapted to provide a signal indicative of the desired clock signal delay in response to at least two consecutive determined phase differences in the same direction.

12. (Original) The apparatus of claim 1, wherein the phase detector is at least one of a latch-type detector, an arbiter-type detector, and a counter-type detector.

13. (Original) The apparatus of claim 1, wherein the second circuit comprises a hysteresis adjuster.

14. – 44. (Cancelled).